1. A method for making stacked metal-insulator-metal (MIM) capacitors on a semiconductor substrate comprising the steps of:

providing said semiconductor substrate having partially completed circuits;

depositing an insulating layer and forming openings for node contacts;

forming said node contacts in said openings;

depositing sequentially a first metal layer, a dummy layer, and a second metal layer on said insulating layer and over said node contacts;

patterning said second metal layer, said dummy layer, and said first metal layer and leaving portions over said node contacts;

depositing a blanket third metal layer on said substrate and over said portions, and etching back to form sidewall spacers on said portions to provide lower electrodes for said capacitors;

depositing a blanket conformal interelectrode dielectric layer (IDL) on said substrate and over said lower electrodes;

depositing a blanket fourth metal layer on said IDL and patterning said fourth metal layer and said IDL to form upper electrodes to complete said MIM capacitors.

2. The method of claim 1, wherein said insulating layer is silicon oxide deposited by chemical vapor deposition to a thickness of between about 3000 and 12000 Angstroms.

3. The method of claim 1, wherein said node contacts are formed by depositing a polysilicon layer sufficiently thick to fill said openings and polishing back to said insulating layer.

4. The method of claim 1, wherein said first metal layer is selected from the group that includes titanium nitride, tungsten nitride, tantalum nitride, titanium, and tungsten.

5. The method of claim 1, wherein said first metal layer is a transition metal selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 1000 Angstroms.

6. The method of claim 1, wherein said dummy layer is deposited to a thickness of between about 2000 and 12000 Angstroms.

7. The method of claim 6, wherein said dummy layer is an insulating material selected from the group that includes silicon oxide, spin-on glass, doped spin-on glass, nitride, and silicon oxynitride.

8. The method of claim 1, wherein said second metal layer is selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 600 Angstroms.

9. The method of claim 1, wherein said blanket third metal layer is selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 1000 Angstroms.

10. The method of claim 1, wherein said blanket conformal interelectrode dielectric layer is selected from the group that includes strontium titanate, barium strontium titanate, and PZT and is formed to a thickness of between about 10 and 500 Angstroms.

11. The method of claim 1, wherein said blanket fourth metal layer is selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 1200 Angstroms.

12. A method for making stacked metal-insulator-metal (MIM) capacitors on a semiconductor substrate comprising the steps of:

providing said semiconductor substrate having partially completed circuits;

depositing an insulating layer and forming openings for node contacts;

forming said node contacts in said openings;

depositing a first metal layer on said insulating layer and over said node contacts;

depositing a dummy layer on said first metal layer, said dummy layer composed of an insulating material;

depositing a second metal layer on said dummy layer;

patterning said second metal layer, said dummy layer, and said first metal layer and leaving portions over said node contacts;

depositing a blanket third metal layer on said substrate and over said portions, and etching back to form sidewall spacers on said portions to provide lower electrodes for said capacitors;

depositing a blanket conformal interelectrode dielectric layer (IDL) on said substrate and over said lower electrodes;

depositing a blanket fourth metal layer on said IDL and patterning said fourth metal layer and said IDL to form upper electrodes to complete said capacitors.

13. The method of claim 12, wherein said insulating layer is silicon oxide deposited by chemical vapor deposition to a thickness of between about 3000 and 12000 Angstroms.

14. The method of claim 12, wherein said node contacts are formed by depositing a polysilicon layer sufficiently thick to fill said openings and polishing back to said insulating layer.

15. The method of claim 12, wherein said first metal layer is a transition metal selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 1000 Angstroms.

16. The method of claim 12, wherein said dummy layer composed of said insulating material is deposited to a thickness of between about 2000 and 12000 Angstroms.

17. The method of claim 16, wherein said insulating material is selected from the group that includes silicon oxide, spin-on glass, doped spin-on glass, nitride, and silicon oxynitride.

18. The method of claim 12, wherein said second metal layer is selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 600 Angstroms.

19. The method of claim 12, wherein said blanket third metal layer is selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 1000 Angstroms.

20. The method of claim 12, wherein said blanket conformal interelectrode dielectric layer is selected from the group that includes strontium titanate, barium strontium titanate, and PZT, and is formed to a thickness of between about 10 and 500 Angstroms.

21. The method of claim 12, wherein said blanket fourth metal layer is selected from the group that includes platinum, ruthenium, and iridium, and is deposited to a thickness of between about 100 and 1200 Angstroms.

22. A stacked metal-insulator-metal (MIM) capacitor on a semiconductor substrate comprised of:

said semiconductor substrate having partially completed circuits;

an insulating layer having openings with node contacts in said openings;

portions of a patterned stacked layer formed from a lower first metal layer, a dummy layer comprised of an insulating material, and an upper second metal layer, said portions over and contacting said node contacts;

sidewall spacers formed form a third metal layer on said portions of said stacked layer for capacitor lower electrodes;

an interelectrode dielectric layer (IDL) on said lower electrodes;

upper electrodes comprised of a patterned fourth metal layer over said lower electrodes.

23. The structure of claim 22, wherein said insulating layer is silicon oxide having a thickness of between about 3000 and 12000 Angstroms.

24. The structure of claim 22, wherein said node contacts are a material selected from the group that includes polysilicon, tungsten, and a combination thereof.

25. The structure of claim 22, wherein said lower first metal layer is selected from the group that includes titanium nitride, tungsten nitride, tantalum nitride, titanium, and tungsten, and said upper second metal layer is selected from the group that includes platinum, ruthenium, and iridium, and have a thickness of between about 100 and 1000 Angstroms.

26. The structure of claim 22, wherein said dummy layer comprised of said insulating material is selected from the group that includes silicon oxide, spin-on glass, doped spin-on glass, nitride, and silicon oxynitride, and has a thickness of between about 2000 and 12000 Angstroms.

27. The structure of claim 22, wherein said third metal layer is selected from the group that includes platinum, ruthenium, and iridium, and said sidewall spacers have a thickness of between about 100 and 1000 Angstroms.

28. The structure of claim 22, wherein said interelectrode dielectric layer is selected from the group that includes strontium titanate, barium strontium titanate, and PZT, and has a thickness of between about 10 and 500 Angstroms.

29. The structure of claim 22, wherein said fourth metal layer is selected from the group that includes platinum, ruthenium, and iridium, and has a thickness of between about 100 and 1200 Angstroms.